Logarithmic pulse generator for long-term creep and relaxation testing

Ashish L. Oza[a] and Ronald P. McCabe
Orthopedic Research Laboratories, Department of Orthopedics and Rehabilitation, University of Wisconsin, Madison, Wisconsin 53792

Ray Vanderby
Orthopedic Research Laboratories, Department of Orthopedics and Rehabilitation, Department of Biomedical Engineering, and Department of Engineering Physics, University of Wisconsin, Madison, Wisconsin 53792

Roderic S. Lakes
Department of Biomedical Engineering, and Department of Engineering Physics, University of Wisconsin, Madison, Wisconsin 53706

(Received 15 October 2004; accepted 24 February 2005; published online 20 April 2005)

An existing logarithmic time base pulse generator design has been modified to collect data for creep and relaxation tests over at least 14 decades of logarithmic time increments. Creep and relaxation studies of materials, which do not obey time temperature superposition, are done over many factors of ten (decades) of time. To acquire and store data efficiently one employs logarithmic sampling intervals. This device can trigger a data acquisition system to gather the data logarithmically. It generates trigger pulses accurately over 14 decades of time. © *2005 American Institute of Physics.* [DOI: 10.1063/1.1897667]

Viscoelasticity is the time dependent behavior of a material, in contrast to elasticity, which is time independent. Creep and relaxation are two important transient properties of a viscoelastic material. In creep, stress is held constant and strain increases with time. In relaxation, strain is held constant and stress decreases with time. Results of viscoelastic transient experiments are usually plotted versus log time. A wide range of log time is desirable because even a single-relaxation-time process, described by an exponential in the time domain, occupies about one decade (factor of 10). Most viscoelastic properties occur over a broader range. For some polymers one can obtain a wide range of effective time via time-temperature superposition, but for composites and biological materials this is not applicable, therefore it is desirable to conduct experiments over a wide range of real time. Collection of data over many decades of time using a linear scale is problematical due to the large number of points required and the unnecessary concentration of points at the short end of the time scale. It would then be very useful to have a method to trigger data acquisition at logarithmic time intervals.

Several logarithmic time base pulse generator designs have been developed and reported.[1–5] For example a prior design[1] provides 7 decades, but we often seek 11 decades of transient and dynamic characterization in our laboratory. This article describes a modification to increase the pulser's range of operation to 14 decades. IC 14536 has a maximum limit of dividing the pulse frequency by 2^{24} [7.2 decades (factors of 10)]. Authors in Ref. 1 used only one frequency divider [integrated circuit (IC) 14536] and mentioned that using more frequency dividers (IC 14536) would extend the number of decades to be covered. To achieve a higher range of time, circuit requires: (a) 1st frequency divider should divide the pulse frequency starting from 2^1 to 2^{24}, (b) 1st frequency divider should hold the frequency division at 2^{24} when it reaches that point and at the same time enable the 2nd frequency divider to continue the frequency division. Designing the circuit to function in the above manner was accomplished and a number of other active and passive components had to be added to make a smooth transition from one frequency divider to another. Our design offers the flexibility of selecting the timing between the first two pulses from as low as 8 μs to over 30 s, (via jumper settings), thus allowing for testing materials via test apparatus with different rise times.

A simplified block diagram of the circuit is shown in Fig. 1. A detailed circuit diagram can be found at the following web address: http://silver.neep.wisc.edu/~lakes/LogCreepFig1.gif. The primary integrated circuits of this design are ICs 2 and 7 (MC14536) and ICs 3 and 8 (CD4040B). Complementary-metal-oxide-semiconductor (CMOS) digital IC MC14536 is a programmable 24-stage binary ripple counter with 16 stages selected by a binary input code. It can divide the frequency of either its on-chip oscillator or an external clock by 2^{N+1}, where N is determined by the address inputs (ABCD) as shown in Fig. 1. Since it has 24 flip-flop stages, it can divide the input frequency from 2^1 (2) to 2^{24} (1.67^*10^7), therefore operating over 7.2 decades (factors of 10) of time.[6] By selecting the appropriate counter stage with the appropriate input clock frequency, a wide variety of timing pulses can be achieved.[6]

The CD4040B IC is a 12-stage ripple carry binary counter in which the counter is advanced on the negative transition of each input clock pulse (Cin).[7] The output lines of the CD4040B (Q1–Q5) are connected to the address inputs of IC MC14536 (A, B, C, D, and Bypass). So each increment in the count of the IC CD4040B halves the output frequency of the MC14536.

[a]Author to whom correspondence should be addressed; electronic mail: oza@orthorehab.wisc.edu

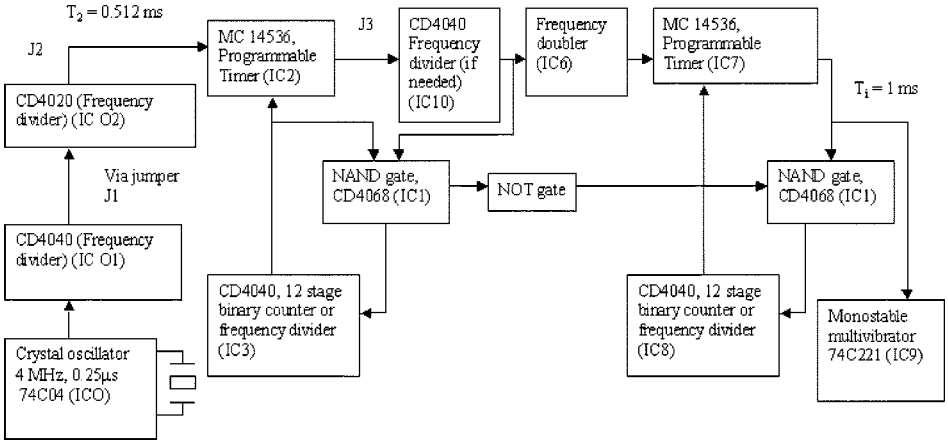

FIG. 1. Block diagram of a logarithmic pulse generator. Detailed circuit diagram can be found at the following link: http://silver.neep.wisc.edu/~lakes/LogCreepFig1.gif.

In this design, a 4 MHz crystal oscillator (IC O) continuously sends out pulses to IC O2 (CD4020B) (binary counter) via IC O1 (CD4040B). Based on the desired output time between two pulses, the appropriate pin of IC O2 is connected to the input of the programmable timer IC2 shown in Table I. When a first trigger pulse 0.5 ms apart from the next pulse enters the IC2, its frequency gets divided by 2^1. This sets the pulses at the output of IC2, 1 ms apart from each other. The frequency then gets multiplied by 2 because of IC6, which is a frequency doubler. So pulses are again separated by 0.5 ms at the output of IC6. IC7, a frequency divider which divides the frequency by 2. So pulses are set apart at 1 ms at the output of second timer (IC7). Since the MC14536 divides the frequency by a minimum of 2^1 and two MC14536's are used, we also need a frequency multiplier in the circuit that multiplies the frequency by 2. This is so that a time (Ti) of 1 ms is obtained between first two pulses at the output of the 2nd timer (IC7) when the first two pulses are 0.5 ms apart at the input of the first timer (IC2) as shown in Table I. Pin 15 of IC O2 is connected (via jumper J2) to the input clock pin of IC2 to obtain a timing of 0.5 ms between the first two pulses. IC2 has 24 flip-flop stages so the input frequency can be divided from 2^1 to 2^{24} based on the stage selected. Therefore, if the second flip-flop stage is selected, the input frequency is divided by 2^2, and if the 20th flip-flop stage is selected, the input frequency is divided by 2^{20}. Selection of a stage in IC2 is decided by the address inputs that come from the outputs of IC3 based on the truth table of MC14536.[6] An increment in the pulse count changes the logic of output lines (Q_1, Q_2, Q_3, Q_4 and Q_5) of CD4040 (IC3 and IC8). Logic of address lines of the timer chips (IC2 and IC7) changes as the address lines are connected to the output lines of CD4040 (IC3 and IC8). Change in the logic of the address line changes the stage of the flip-flop selected and frequency of the pulse entering IC2 and IC7 gets divided by 2^N where N is the stage of the flip-flop selected.

In this design another programmable timer (IC7) is cascaded after the first timer (IC2) to extend the range of the pulse generator. The first timer (IC2) starts dividing the oscillator frequency as the number of its output pulses starts increasing. When the 24th negative going edge arrives at timer IC3, it divides the frequency by 2^{24}, after which, all the address inputs of IC2 are held at logic high (via IC4 and IC1c). IC7 will then be enabled and will continue dividing the oscillator frequency by 2^{25}, and the second timer (IC7) repeats the whole process of frequency division. Thus, the 7 decade time range attainable using a single timer is extended to 14 decades. IC9 (74C221) provides an adjustable

TABLE I. Table showing pin number of ICO2 (CD4020B) connected to IC2(MC14536), which determines the frequency division (2^n), time between first two trigger pulses going into the first timer, time (Ti) between first two pulses at the output of the 2nd timer (IC7).

Pin	n	2^n	Frequency (Hz) of trigger pulses into the 1st timer (IC2)	Time (ms) between two trigger pulses into the 1st timer	Time between two consecutive pulses (Ti) in ms at the output of IC7
7	4	16	250 000	0.004	0.008
5	5	32	125 000	0.008	0.016
4	6	64	62 500	0.016	0.032
6	7	128	31 250	0.032	0.064
13	8	256	15 625	0.064	0.128
12	9	512	7813	0.128	0.256
14	10	1024	3906	0.256	0.512
15	**11**	**2048**	**1953**	**0.512**	**1.024**
1	12	4096	977	1.024	2.048
2	13	8192	488	2.048	4.096
3	14	16 384	244	4.096	8.192

(via R and C) precision output pulse to trigger the data acquisition system. The width of the pulses coming out of IC9, in our case, was fixed to 1 ms. Five pulses of amplitude 10 V into 1 M Ω are provided in the first 50 ms.

This design covers over 14 decades of time. In the present embodiment there are 3–4 points per decade (depending on the decade), for the following reason. The first trigger pulse entering IC2 is 1 ms apart from the next pulse. Due to the frequency division caused by the two timer chips and frequency doubling caused by IC6, pulses at the output of IC7 will appear at 2 ms… 64 ms, 128 ms, 256 ms, 512 ms, 1024 ms, 2048 ms, 4096 ms, 8192 ms, etc. So there are three points between 100 and 1000 ms and four points between 1000 and 10 000 ms. IC10 (CD4040B) and jumper J3 allow one to specify more pulses per decade of time. Setting J3, on IC10, to allow more pulses per decade requires changing J2 (or J1) to speed up the clock (for constant initial pulse time). IC6a is a simple frequency doubler to make up for the fact that IC2 will not divide by 2^0. A "Power-on Reset" circuit initializes all counters and flip-flops to a known stable state. This is necessary due to the flip flops, which are not designed to power-on in any particular state. "Auto Start In" is an optional input allowing the test machine to trigger the pulse generator and is connected to the testing machine via a cable. The "Start/Stop" switch is a three position switch (momentary-off-momentary) that allows the user to start the pulse generator and to start the test machine and hence the test. The Start/Stop switch is left in the neutral position when used in the "Automatic trigger" mode. "Run out" is connected to the testing machine via a cable to trigger the testing machine. A battery backup feature allows the counter to continue to operate, if there is a temporary main power loss. The time between two initial pulses at the output of IC7 in our circuit is set at 1 ms and, as seen in Table I, the lowest limit in time duration possible between two initial pulses is 8 μs.

A microprocessor could be used to design a logarithmic pulse generator, but the level of complexity in its software design might be the same as the level of complexity in our hardware design. One would also need access to a compiler, or assembler, and hardware to program the microprocessor.

In summary, we designed and implemented a logarithmic time base pulse generator keeping two things in mind (1) to allow an arbitrarily long range of time covered by the pulse generator and (2) to easily set the initial pulse time for determining the material properties of materials using test devices with different rise times.

The author would like to thankfully acknowledge the NSF Grant No. CMS 9907977 and the Department of Orthopedics and Rehabilitation, University of Wisconsin—Madison.

[1] E. F. Denby and L. J. Wills, Rev. Sci. Instrum. **49**, 267 (1978).
[2] W. N. Trump and L. Fowler, Rev. Sci. Instrum. **45**, 714 (1974).
[3] L. J. Wills and E. F. Denby, Rev. Sci. Instrum. **46**, 1030 (1975).
[4] R. H. Austin, K. W. Beeson, S. S. Chan, P. G. Debrunner, R. Downing, L. Eisenstein, H. Frauenfelder, and T. M. Nordlund, Rev. Sci. Instrum. **47**, 445 (1976).
[5] L. J. Wills and N. G. Ly, Rev. Sci. Instrum. **56**, 2157 (1985).
[6] MC14536B data sheet, Rev. 7, (2001). (ON Semiconductor—http://www.onsemi.com/pub/Collateral/MC14536B-D.PDF).
[7] *CMOS Databook* (National Semiconductor, 1977).